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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P9486 Total Pages 2

First Named Inventor or Application Identifier Thomas G. Ruttan

Express Mail Label No. EL627464499US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 17)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 4)

4. X Oath or Declaration (Total Pages 6)(Unsigned)
   a. ___ Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. __ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. __ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. __ Assignment Papers (cover sheet & documents(s))
9. __ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__ b. Power of Attorney
10. __ English Translation Document (if applicable)
11. __ a. Information Disclosure Statement (IDS)/PTO-1449
__ b. Copies of IDS Citations
12. __ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. __ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. __ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. X Other: Express Certificate of Mailing

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
____ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _

18. **Correspondence Address**
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Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL FOR FY 2000

TOTAL AMOUNT OF PAYMENT ($) 690.00

Complete if Known:
Application No. New Application
Filing Date Herewith
First Named Inventor Thomas G. Ruttan
Group Art Unit Not yet assigned
Examiner Name Not yet assigned
Attorney Docket No. 042390.P9486

METHOD OF PAYMENT (check one)

1. [ ] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

Deposit Account Number 02-2666
Deposit Account Name

[X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

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2. X **Payment Enclosed:**
X **Check**
____ **Money Order**
____ **Other**

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility application filing fee	690.00
106	310	206	155	Design application filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 690.00

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	18	– 20** =	0	X	= 0.00
Independent Claims	3	– 3** =	0	X	= 0.00
Multiple Dependent					=

****Or number previously paid, if greater; For Reissues, see below.**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 0.00

Patent fees are subject to annual revisions. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid.
See Forms PTO/SB/09-12

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,210	241	605	Petition to revive unintentionally abandoned application	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	
Other fee (specify)					
Other fee (specify)					

SUBTOTAL (3) $ 0.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Michael A. Bernadicou

Signature [signature] Date 9/28/00

Reg. Number 35,934 Deposit Account User ID 02-2666 (complete if applicable)

APPLICATION FOR UNITED STATES LETTERS PATENT

SYSTEM AND METHOD FOR CONNECTING A POWER CONVERTER TO A LAND GRID ARRAY SOCKET

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Docket No. 042390.P9486

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September 28, 2000
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SYSTEM AND METHOD FOR CONNECTING A POWER CONVERTER TO A L AND GRID ARRAY SOCKET

FIELD OF THE INVENTION

The present invention relates generally to power delivery for electronic circuits and, more particularly, to an improved power connector for land grid array (LGA) central processing unit (CPU) sockets.

BACKGROUND

A standard computer system typically includes integrated circuit devices mounted to a large printed circuit board known as a motherboard using a socket or similar type of electrical connector. The motherboard is supplied with voltage from a power supply, usually at a higher DC level than is required by the integrated circuit device.

Currently, a voltage regulator (i.e., a DC-DC converter) is used in certain high performance computer systems along with a pin grid array (PGA) socket. The central processing unit (CPU) package that connects to the socket consists of an integrated circuit device (e.g., a silicon chip) soldered to a package substrate using flipchip ball grid array (FCBGA) which, in turn, is soldered to one side of an interposer using ball grid array (BGA) technology. The package substrate connects to the PGA socket using multiple contacts in a matrix arrangement each having a pin type tail. The DC-DC converter connection consists of a multi-layer flex board and an edge-card connector that connects to one edge of the interposer substrate. The present configuration requires the CPU package to be inserted into the PGA socket in the vertical axis (i.e., the Z-axis). The DC-DC converter is then attached in the X-axis sliding direction requiring a complex retention mechanism.

In the recently developed land grid array (LGA) socket an array of pads, rather than pins, provide the requisite electrical connections between the integrated circuit device and the printed circuit board. LGA sockets are advantageous because they do not require soldering between the socket and the CPU package. Moreover, LGA sockets reduce the height of the socket/package/CPU solution (because they do not require the use of long pins) thereby resulting in shorter circuit paths and improved electrical performance. However, in order to connect the current DC-DC converter to an LGA socket, an interposer would be required to provide the edge-card interface required by the DC-DC converter. The interposer would add height, electrical path length, and parasitic inductance to the socket/package/CPU solution, thus negating the advantages of using the LGA socket.

Although multiple one ounce copper power planes may also be used to supply power from the DC-DC converter to the CPU socket through the motherboard, an excessive number of power and ground contacts would be needed and the additional power and ground planes make motherboard routing difficult. Delivering high DC currents through the motherboard to the LGA socket is an expensive solution and has additional technical challenges not associated with delivering current directly onto the LGA socket assembly.

Therefore, it would be advantageous to provide a low inductance and resistance interconnect that improves the current carrying capacity from the DC-DC converter to the LGA socket. It would also be helpful if the interconnect required only a single direction (vertical or Z-axis) of assembly which would save time and manufacturing costs.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements and which:

Figure 1A is a top view of an unassembled LGA integrated circuit device package and a DC-DC converter according to one embodiment of the present invention.

Figure 1B is a top view of an assembled LGA integrated circuit device package and a DC-DC converter according to one embodiment of the present invention.

Figure 2 is an exploded view of a cross section of the contact details of a DC-DC converter as it is being mounted to a power socket interface according to one embodiment of the present invention.

Figure 3 is an exploded view of a cross-section of the contact details of an LGA socket mounted to a motherboard according to one embodiment of the present invention.

Figure 4A is a cross-sectional view of the spatial relationship of the component parts of an unassembled LGA integrated circuit device package and a DC-DC converter according to one embodiment of the present invention.

Figure 4B is a cross-sectional view of the spatial relationship of the component parts of an assembled LGA integrated circuit device package and a DC-DC converter according to one embodiment of the present invention.

DETAILED DESCRIPTION

Throughout the following description specific details are set forth in order to provide a more thorough understanding of the invention. However, the invention may be practiced without these particulars. In other instances, well known elements have not been shown or described in detail to avoid unnecessarily obscuring the present invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

Compression contact technology has been used in the computer industry for a number of years. Various forms of this technology have been developed, including polymer based contacts with electrically conductive metal particles or wires imbedded in the polymer and stamped metal contact springs. For example, there are commercially available sockets, connectors, and interconnect products using this technology. However, compression contact technology has never been employed to connect a voltage regulator (i.e., a DC-DC converter) to a land grid array (LGA) socket.

It would be helpful to use compression contacts (e.g., metal, conductive polymer, or others) to eliminate the edge-card connector typically used in this application, thus reducing the loop inductance and contact resistance of the connection. Furthermore, compression contacts would simplify the retention and mounting mechanism of the LGA socket by providing a means for contacting the LGA socket from a vertical rather than a horizontal direction as is required using conventional edge-card connectors.

The present embodiment provides a power connector consisting of a circuit board connected to one end of a DC-DC converter output circuit board. Since the connector must carry very high current levels from the DC-DC converter to the LGA socket and

return (ground), these connections on the circuit board consists of one or more layers each of wide and thick metal, such as four ounce or six ounce copper. The compression contacts may be attached at the other end of the board with sufficient numbers and cross-sectional area to carry the required electrical current. The board may be mated to the LGA socket with the appropriate contact pattern and the contacts may be compressed with a clamping or retention mechanism. The retention mechanism provides the clamping force as well as the compression stop so that the contacts will be compressed to a predetermined level, but will not continue to compress further. The LGA socket has the required metal conductor layers to carry the electrical current from the power contacts and to the CPU.

Referring now to Figure 1A, there is shown a top view of an unassembled LGA integrated circuit device package and a DC-DC converter 100 in accordance with an embodiment of the present invention. An integrated circuit device 110 (i.e., a silicon chip) may be mounted to an LGA package 120 in a manner well known in the art of microelectronic fabrication. The LGA package 120 comprises a substrate which may be fabricated of laminates such as FR-4, fiberglass or bismaleimide-triazine (BT) material, of coated aluminum, ceramic, or other suitable materials and multiple conductive layers which are laminated or co-fired between the varied dielectric layers. The integrated circuit device 110 may be an analog device, a microprocessor, an application specific device, or any other type of integrated circuit device and may be electrically connected to an array of terminals (i.e., typically circular or rectangular pads) (not shown in this view) on the LGA package 120. The pads on the LGA package 120 correspond to a pattern of

a contact array (not shown in this view) on an LGA socket 130 when properly aligned with the socket 130.

The socket itself 130 is sandwiched between the LGA package 120 and the motherboard (not shown in this view). The socket 130 comprises a substrate formed of non-conductive material to receive the LGA package 120. The contacts on the socket 130 may be fabricated of a conductive material and extend transversely through the substrate from a top surface of the substrate to a bottom surface of the substrate. The contacts function to electrically couple the socket 130 and the LGA package 120 to the underlying motherboard on which the socket 130 is mounted. The socket 130 may be mated to the motherboard by a force applied downwardly on the socket 130 which then compresses the conductive elements to effect a reliable electrical contact between the socket 130 and its respective contact pads and the motherboard and its respective contact pads. In order to maintain alignment between the pads, a retention mechanism such as a frame element (now shown in this view) may be provided around the socket 130. In addition, a spring clip extending across the body of the frame element or any other suitable clamping mechanism may be used to hold the socket 130 down against the pads on the motherboard. Of course, it should be noted that the socket 130 may also be soldered down (surface mounted) to the motherboard using conventional reflow soldering methods or mounted to the motherboard using a variety of other techniques well known in the art.

An LGA power socket interface 140 comprising an array of contact pads 142, 144, 146, etc., existing on one side of the power socket interface 140 function to connect the power socket interface 140 to the DC-DC converter 150. The power socket interface

140 may be part of the socket 130 or, alternatively, may exist as a separate contact arrangement (not shown in this view). The contact pads 142, 144, 146, etc., may be fabricated from metal, conductive polymer, or any other suitable material. The contact pads 142, 144, 146, etc., on the power socket interface 140 correspond to an array of contact pads 152, 154, 156, etc., existing on the DC-DC converter 150. The number and arrangement of the power contact pads 142, 144, 146, 152, 154, 156, etc., is such that the resistance and inductance of the interconnect is minimized. The patterns to minimize inductance are well known to those skilled in the art of the fabrication of microelectronic packages. The two devices may thus be mated together using compression contact technology in the same manner as is previously described. Alignment apertures 162 and 164 on the power socket interface 140 and alignment apertures 166 and 168 on the DC-DC converter 150 help ensure proper alignment between the power socket interface 140 and the DC-DC converter 150 (i.e., when the two devices are compression mounted alignment pins (not shown in this view) are inserted into the alignment apertures 162, 164, 166, and 168 to help align the devices). Although alignment pins are described in the present embodiment, other forms of fastening mechanisms are also possible such as spring clips and the like.

The DC-DC converter 150 connects to a power supply (not shown in this view) that supplies power at a higher voltage (e.g., 12 or 48 volts and ground) than is typically required by the integrated circuit device 110. The DC-DC converter 150 includes conventional voltage conversion circuits within a housing to convert the higher voltage to a lower voltage and to supply the lower voltage to the power socket interface 140 and subsequently to the motherboard in a manner well known in the art. A heat sink

comprised of thermally conductive materials (e.g., copper, aluminum, titanium, etc.) may form the outer casing of the DC-DC converter 150 so that heat generated by the conversion circuits can dissipate by convection directly into the surrounding air in a manner well known in the art. It should be noted that by configuring the DC-DC converter 150 in the manner described by the present embodiment, benefits are provided to the manufacturer in that the DC-DC converter 150 may be separately tested before mating the DC-DC converter 150 to the power socket interface 140.

Referring now to Figure 1B, there is shown a top view of an assembled LGA integrated circuit device package and a DC-DC converter 180 in accordance with an embodiment of the present invention. The array of contacts 152, 154, and 156, etc., on the DC-DC converter 150 and an array of contacts (not shown in this view) on a power socket interface 140 are compression mounted together. Alignment pins (not shown in this view) inserted through alignment apertures 166 and 168 in the DC-DC converter 150 and alignment apertures (not shown in this view) in the power socket interface 140 assist in the proper alignment between the two devices. A retention mechanism 170 performs an additional alignment function and maintains the DC-DC converter 150 in secure electrical contact with the power socket interface 140. The retention mechanism 170 may be fabricated from plastic, aluminum, or any other suitable materials. In the present embodiment, the retention mechanism 170 comprises a frame element rectangular in shape that may be secured with nuts and bolts to the motherboard (not shown in this view), although other fastening techniques well known in the art may also be uses. An LGA socket 130 including an LGA package 120 (which includes an integrated circuit device 110) mounted to the socket 130 in a manner well known in the art of

microelectronic fabrication may be mated to the motherboard through a relief (not shown in this view) in the retention mechanism 170. It should be understood, however, that although the retention mechanism 170 is illustrated in the embodiment illustrated by Figure 1B, it is also possible to use the socket 130 itself as a retention mechanism or to use other similar retention mechanisms known in the art.

Referring now to Figure 2, there is shown an exploded view of a cross section of the contact details of a DC-DC converter mounted to a power socket interface 200 in accordance with an embodiment of the present invention. An array of contacts 210, 220, and 230 on the DC-DC converter 240 are compression mounted to an array of contacts 250, 260, and 270 on the power socket interface 280. The DC-DC converter 240 is pressed downward from a vertical direction on to the power socket interface 280, thus providing for a single direction of assembly.

Referring now to Figure 3, there is shown an exploded view of a cross section of the contact details of an LGA socket mounted to a motherboard 300 in accordance with an embodiment of the present invention. The socket base 310 includes an array of contacts 312 and 314, etc., formed to receive corresponding land pads of an LGA package (not shown in this view). The contacts 312 and 314, etc., may be formed of a conductive material (e.g., conductive polymer, metal, or others) and extend from a top surface of the socket base 310 to a bottom surface of the socket base 310 and provide electrical coupling of an integrated circuit device (not shown in this view) to a motherboard 320. Coax structures 322, 324, 326, etc., for high signal integrity may be metalizations of the socket 330 and provide a stop for the socket 330 as it is compressed downward from a vertical direction on to the motherboard 320 so that the contacts 312

and 314, etc., compress to a predetermined level but will not continue to compress further. Copper bar 340 (and multiple other copper bars (not shown in this view)) coupled to the socket base 310 may be used for EMI shielding and/or ground for the integrated circuit device I/0 structure. In the embodiment illustrated by Figure 3, the copper bar 340 and the multiple other copper bars are relatively wide and thick (i.e., six ounces), but copper bars of other dimensions may also be used.

Referring now to Figure 4A, there is shown a cross-sectional view of the spatial relationship of the component parts of an unassembled LGA integrated circuit device package and a DC-DC converter 400 in accordance with an embodiment of the present invention. An integrated circuit device 410 may be connected to an LGA package 420 using an array of terminals (i.e., land pads) 422, 424, 426, etc., in a manner described in the embodiment illustrated by Figure 1A. An array of contacts (not shown in this view) on an LGA socket 430 correspond to the land pads 422, 424, 426, etc., on the LGA package 420. The contacts on the socket 430 may be fabricated from conductive polymer or other suitable material and are coupled to the socket base 440. The contacts comprise compressive contacts to receive electrical signals from the integrated circuit device 410 and compressive contacts 432, 434, 436, and 438, etc., to receive power from a DC-DC converter 450.

The DC-DC converter 450 comprises a substrate 452 which may be fabricated of laminates such as FR-4, fiberglass, coated aluminum, or any other suitable material, an output voltage plane (i.e., a VCC voltage plane) 454 to provide output voltage to the socket 430, and a ground plane (GND) 456 to complete the circuit path in a manner well known in the art of power delivery systems. A GND plane 442 may also be included in

the socket base 440. The LGA integrated circuit device package and DC-DC converter may be assembled (not shown in this view) and mounted to a motherboard 460 using conventional fastening techniques in a manner described in the embodiment illustrated by Figure 1A. A LGA power socket interface 470 may be mounted to the DC-DC converter 450 in a manner also previously described in the embodiment illustrated by Figure 1A.

Referring now to Figure 4B, there is shown a cross-sectional view of the spatial relationship of the component parts of an assembled LGA integrated circuit device package and a DC-DC converter 490 in accordance with an embodiment of the present invention. The component parts of Figure 4B are identical to the component parts of Figure 4A and thus retain the same numeric designations.

Thus, a structure and process for delivering high current low voltage DC power from a DC-DC converter to an LGA socket and corresponding microelectronic packages without passing that current through the underlying motherboard has been described. Although the foregoing description and accompanying figures discuss and illustrate specific embodiments, it should be appreciated that the present invention is to be measured only in terms of the claims that follow.

CLAIMS

1. A power delivery system, comprising:

a power converter; and

a land grid array socket mounted to an array of contacts on a surface of the power converter corresponding to an array of contacts on the land grid array socket.

2. The power delivery system of Claim 1 wherein the array of contacts on the power converter and the array of contacts on the land grid array socket are contact pads fabricated from electrically conductive material.

3. The power delivery system of Claim 1 wherein the land grid array socket is electrically coupled to a printed circuit board and includes an integrated circuit device mounted to a land grid array package.

4. The power delivery system of Claim 1 wherein the power converter converts voltage received from a power supply to a lower voltage and transmits the lower voltage to the land grid array socket.

5. The power delivery system of Claim 1 wherein the land grid array socket is mounted to the power converter and to a printed circuit board using a single direction of assembly and compression contact technology.

6. A power delivery system, comprising:

a power converter;

a printed circuit board; and

a land grid array socket mounted to an array of contacts on a surface of the power converter and on a surface of the printed circuit board using a single direction of assembly.

7. The power delivery system of Claim 6 wherein the array of contacts on the power converter and on the printed circuit board correspond to an array of contacts on the land grid array socket, the array of contacts fabricated from electrically conductive material.

8. The power delivery system of Claim 6 wherein the land grid array socket includes an integrated circuit device mounted to a land grid array package.

9. The power delivery system of Claim 6 wherein the power converter converts voltage received from a power supply to a lower voltage and transmits the lower voltage to the land grid array socket.

10. The power delivery system of Claim 6 wherein the land grid array socket is mounted to the power converter and to the printed circuit board using compression contact technology.

11. A method of mounting a land grid array socket to a power converter, the method comprising:

providing an array of contacts on a surface of the power converter;

providing an array of contacts on a land grid array socket interface corresponding to the array of contacts on the power converter;

mounting the land grid array socket to the power converter by vertically compressing the array of contacts on the land grid array socket interface with the array of contacts on the surface of the power converter.

12. The method of Claim 11 wherein the step of mounting the land grid array socket to the power converter provides an electrical connection between the land grid array socket and the power converter.

13. The method of Claim 11 wherein the land grid array socket includes an integrated circuit device mounted to a land grid array package.

14. The method of Claim 11 wherein the step of mounting the land grid array socket to the power converter further comprises the step of mounting the land grid array socket to a printed circuit board by vertically compressing an array of contacts on the land grid array socket with an array of corresponding contacts on the printed circuit board.

15. The method of Claim 14 wherein the step of mounting the land grid array socket to the printed circuit board provides an electrical connection between the land grid array socket and the printed circuit board.

16. The method of Claim 11 wherein the step of mounting the land grid array socket to the printed circuit board further comprises the step of mounting the land grid array socket to a retention mechanism, the array of contacts on the land grid array socket

mounted to the array of contacts on the printed circuit board through a relief in the retention mechanism.

17. The method of Claim 11 wherein the land grid array socket serves as a retention mechanism to hold the land grid array socket in proper alignment with the printed circuit board and in proper alignment with the power converter.

18. The method of Claim 11 wherein the power converter converts voltage received from a power supply to a lower voltage and transmits the lower voltage to the land grid array socket

ABSTRACT

A land grid array (LGA) socket is connected to a power converter using compression contact technology eliminating the need for an edge-card connector typically required in such applications. The LGA socket is mounted to the power converter in a single direction of assembly (i.e., the vertical axis).

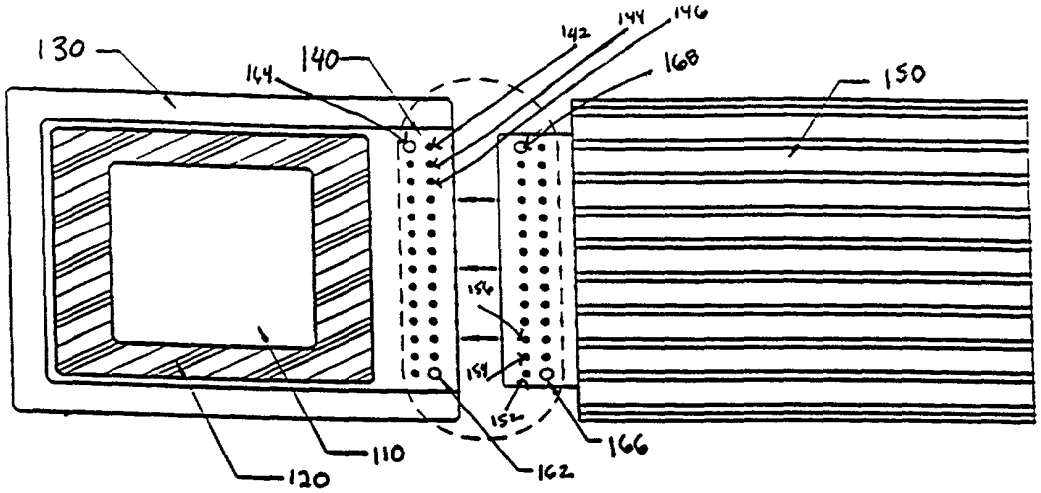

Figure 1A

100 →

TOP VIEW (Unassembled)

Retention/Alignment Not Shown

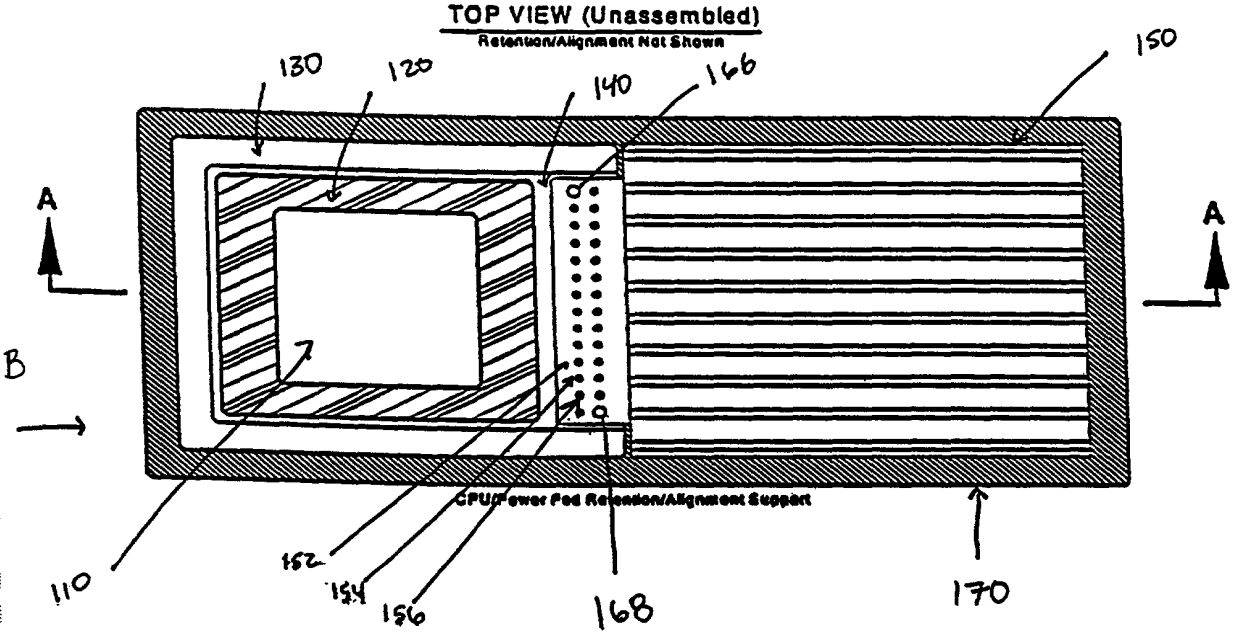

Figure 1B

180 →

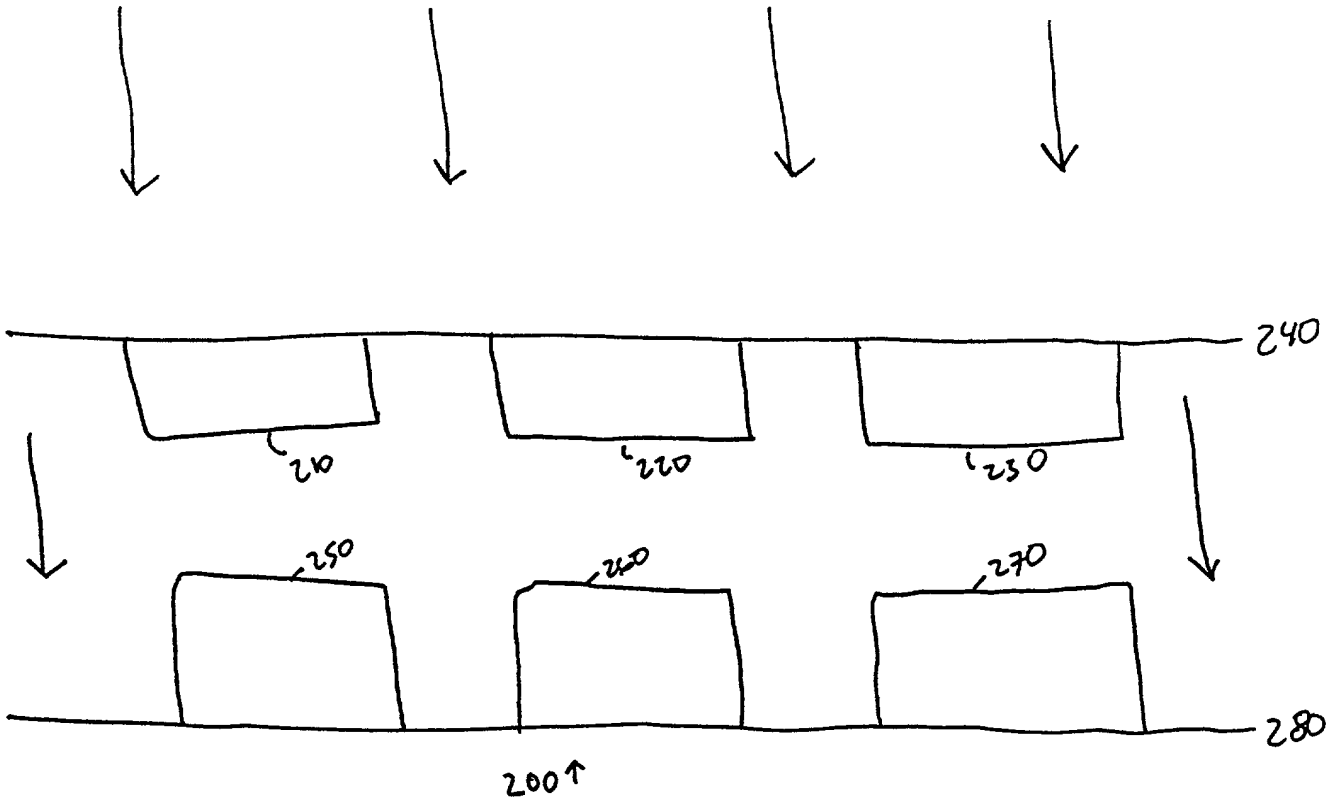

Figure 2

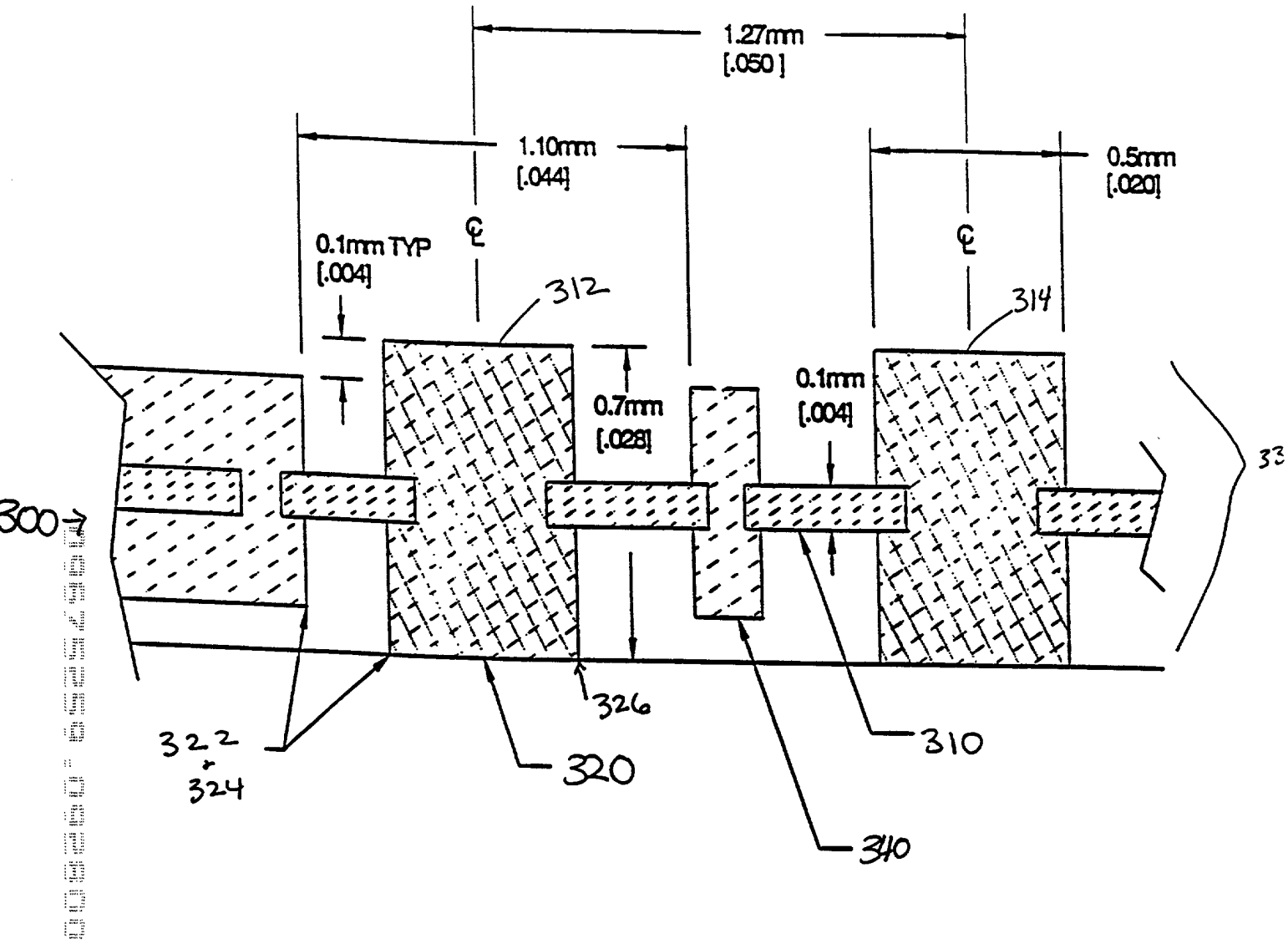
1.27mm
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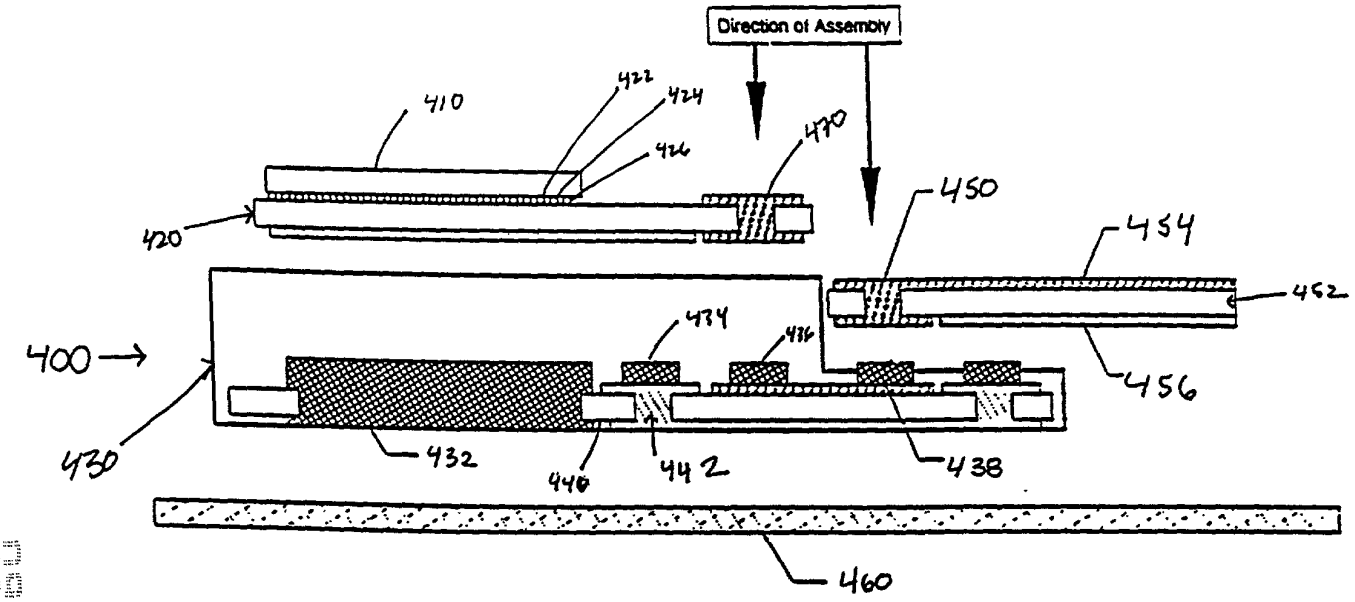
Figure 3

Figure 4A



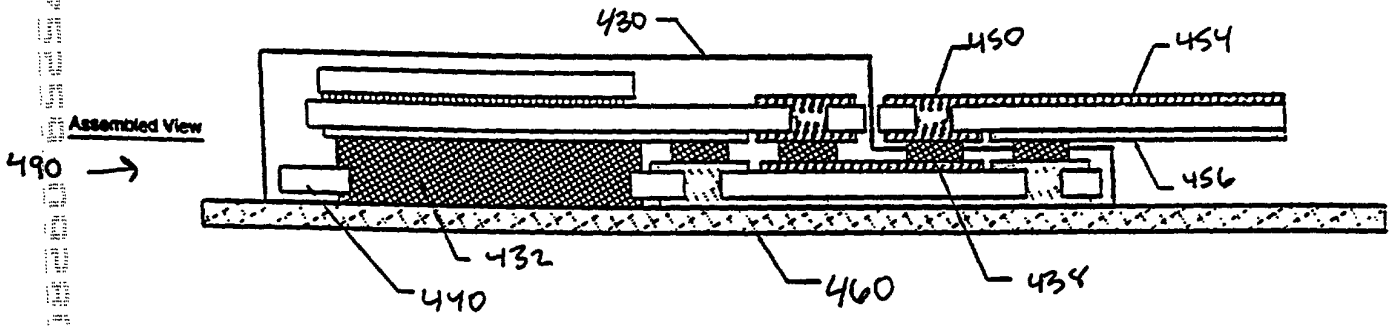


Figure 4B

Attorney's Docket No.: 042390.P9486 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
SYSTEM AND METHOD FOR CONNECTING A POWER CONVERTER TO A LAND GRID ARRAY SOCKET

the specification of which

X is attached hereto.
___ was filed on (MM/DD/YYYY) _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on (MM/DD/YYYY) _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	(Filing Date – MM/DD/YYYY)
Application Number	(Filing Date – MM/DD/YYYY)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	(Filing Date – MM/DD/YYYY)	Status -- patented, pending, abandoned
Application Number	(Filing Date – MM/DD/YYYY)	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Michael A. Bernadicou, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Michael A. Bernadicou, (408) 720-8300.
(Name of Attorney or Agent)
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Sixth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Seventh/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.